The opinion in support of the decision being entered today was *not* written for publication and is *not* binding precedent of the Board.

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte DAVID P. HANNUM and ROHIT BHATIA

Appeal 2006-3434
Application 10/687,907
Technology Center 2100

Decided: March 13, 2007

Before JOSEPH F. RUGGIERO, JOSEPH L. DIXON, and JEAN R. HOMERE, *Administrative Patent Judges*.

HOMERE, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

Appellants appeal from the Examiner's final rejection of claims 1 through 3, 6 through 13, and 16 through 19 pursuant to 35 U.S.C. § 134. We have jurisdiction under 35 U.S.C. § 6(b) to decide this appeal.

The Examiner rejected[1] the claims on appeal as follows:

A. Claims 1, 2, 7, 8, 10 through 12 and 17 through 19 stand rejected under 35 U.S.C. § 102 (b) as being anticipated by Miller.

B. Claims 6, 9 and 16 stand rejected under 35 U.S.C. § 103 (a) as being unpatentable over the combination of Miller and Geva.

C. Claims 3 and 13 stand rejected under 35 U.S.C. § 103 (a) as Miller and Hale.

The Examiner relied on the following references:

Miller	US 5,809,528	Sep. 15, 1998
Geva	US 6,539,541 B1	Mar. 25, 2003
Hale	US 6,564,317 B1	May 13, 2003
Hannum	US 6,823,434 B1	Nov. 23, 2004

Independent claim 1 is illustrative and representative of the Appellants' invention. It reads as follows:

> 1. A method for preventing matching of prospective entries with table entries stored in a fully associative table, the method comprising the steps of:
>
> writing illegal values to substantially all of said table entries in said fully associative table; and
>
> prohibiting said prospective entries from having said illegal values under normal program execution conditions, thereby preventing any matching conditions between said table entries and said prospective entries.

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1 The Examiner also rejected claims 1-3, 6-13 and 16 through 18 under the judicially created doctrine of obviousness double patenting as being unpatentable over claims 1-16 of Hannum.

Appellants contend that Miller does not teach the invention as set forth in claims 1, 2, 7, 8, 10 through 12 and 17 through 19.[2] Particularly, Appellants contend that Miller does not fairly teach or suggest writing illegal values to substantially all the table entries in a fully associative table. (Br. 6; Reply Br. 2-4). For these same reasons, Appellants conclude that claims 3, 6, 9, 13, and 16 are not unpatentable over Miller in combination with Geva or Hale. Appellants further contend that the Examiner has failed to establish sufficient motivation to combine Miller with Geva or Hale.

The Examiner, in contrast, contends that Miller teaches the claimed writing of illegal values in table entries as valid status bits that are initialized to an invalid state (Answer 11). Further, the Examiner contends that it would have been obvious to incorporate Geva's teaching of a most recent advanced load instruction for a check instruction or Hale's teaching of a specific machine for executing writing instructions in Miller's architecture for implementing invalid data (Answer 10).

We affirm.

ISSUES

The pivotal issues in the appeal before us are as follows:

(1) Under 35 U.S.C. § 102 (b), does Miller anticipate the claimed invention when Miller discloses initializing all valid status bits to an invalid state?

(2) Under 35 U.S.C. § 103 (a), would one of ordinary skill in the art at the time of the present invention, have found that sufficient motivation to

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[2] This decision considers only those arguments that Appellants submitted in the Appeal and Reply Briefs. Arguments that Appellants could have made but chose not to make in the Briefs are deemed to have been waived. *See* 37 CFR 41.37(c)(1) (vii)(eff. Sept. 13, 2004). *See also In re Watts*, 354 F.3d 1362, 1368, 69 USPQ2d 1453, 1458 (Fed. Cir. 2004).

combine Geva or Hale with Miller by incorporating a most recent advanced load instruction for a check instruction or a specific machine for executing writing instructions in an architecture for implementing invalid data?

FINDINGS OF FACT

We find that Appellants have elected not to appeal the Examiner's rejection of claims 1-3, 6-13, 16-18 under the judicially doctrine of obviousness double patenting as being unpatentable over claims 1-16 of Hannum.

Appellants invented a method and system (fig. 3) for preventing matches of prospective value entries with illegal entries[3] in a fully associative table (206). Particularly, at initialization, a force update command (203) resulting from a power on condition or a machine specific instruction populates the associative table (206) with illegal entry values. (Specification 11). Thus, any subsequent comparison of illegal value entries in the associative table (206) with prospective value entries received from check instructions (209) will result in a miss (i.e. no match.) Id.

Miller teaches an architecture (fig.1) for implementing an invalid data handling least recently used replacement mechanism in a cache memory system. (Abstract.) Particularly Miller discloses a centrally located address comparator (ACAM) (104) that contains no valid addresses at initialization after initializing all valid status bits to an invalid state. As a result, any comparison of prospective address entries with invalid entry bits in the ACAM will generate a "miss" in the cache memory. Upon the occurrence

[3] Appellants' Specification, at page 8, attempts to "generally" define illegal entries as a value which a prospective entry would preferably not acquire in a normal course of program execution. We find this to fall short of an express definition, but will adopt it in our discussion above.

of a miss, the requested data is placed in the data array and the corresponding system address is placed in of the ACAM, setting one or more valid status bits to the valid state (col. 15, ll. 42-59). Miller also teaches an invalidation operation to invalidate an entry in the ACAM (104). (col. 16, lls 11-18).

Geva teaches a system for optimizing computer software through construction and unrolling of counted loops. (col. 1, ll. 18-24). Particularly, Geva teaches an advanced load address table (ALAT) that interacts with an advance load or advance load check causing the processor to perform a load from a memory location. The ALAT acts as a cache of the physical memory address and the physical register address accessed by the most recently executed advance load. (col. 14, ll. 15-31). During each memory store, store instructions cause the processor to search all entries in the ALAT. All entries in overlapping regions of memory are invalidated. (col. 14, ll. 32-47).

Hale teaches a method for securely invalidating portion of a cache following a write back invalidate instruction during initialization. (col. 9, lines 30-45). Particularly, Hale discloses preventing unlocking of nonvolatile memory during such initialization. Further, Hale indicates that performance of initialization and security functions are vital to ensure the security and integrity of the computer system. Therefore, they must be protected. (col. 1, ll. 24-36).

PRINCIPLES OF LAW

1. ANTICIPATION

It is axiomatic that anticipation of a claim under § 102 can be found only if the prior art reference discloses every element of the claim. *See In re King*, 801 F.2d 1324, 1326, 231 USPQ 136, 138 (Fed. Cir. 1986) and

Lindemann Maschinenfabrik GMBH v. American Hoist & Derrick Co., 730 F.2d 1452, 1458, 221 USPQ 481, 485 (Fed. Cir. 1984).

In rejecting claims under 35 U.S.C. § 102, a single prior art reference that discloses, either expressly or inherently, each limitation of a claim invalidates that claim by anticipation. *Perricone v. Medicis Pharmaceutical Corp.*, 432 F.3d 1368, 1375-76, 77 USPQ2d 1321, 1325-26 (Fed. Cir. 2005), citing *Minn. Mining & Mfg. Co. v. Johnson & Johnson Orthopaedics, Inc.*, 976 F.2d 1559, 1565, 24 USPQ2d 1321, 1326 (Fed. Cir. 1992). Anticipation of a patent claim requires a finding that the claim at issue "reads on" a prior art reference. *Atlas Powder Co. v. IRECO, Inc.*, 190 F.3d 1342, 1346, 51 USPQ2d 1943, 1945 (Fed Cir. 1999) ("In other words, if granting patent protection on the disputed claim would allow the patentee to exclude the public from practicing the prior art, then that claim is anticipated, regardless of whether it also covers subject matter not in the prior art.") (internal citations omitted).

2. OBVIOUSNESS

On appeal, Appellants bears the burden of showing that the Examiner has not established a legally sufficient basis for combining the teachings of the references that the Examiner relied upon. Appellants may sustain this burden by showing that the Examiner failed to provide sufficient evidence to support that one having ordinary skill in the art would have combined disclosures of the references, as proposed by the Examiner, to yield Appellant's invention. *United States v. Adams*, 383 U.S. 39 (1966); *In re Kahn*, 441 F.3d 977, 987-988, 78 USPQ2d 1329, 1336 (Fed. Cir. 2006); *DyStar Textilfarben GmbH & Co. Deutschland KG v. C.H. Patrick, Co.*, 464 F.3d 1356, 1360-1361, 80 USPQ2d 1641, 1645 (Fed. Cir. 2006). The mere

fact that all the claimed elements or steps appear in the prior art is not *per se* sufficient to establish that it would have been obvious to combine those elements. *United States v. Adams*, *supra*; *Smith Industries Medical systems, Inc. v. Vital Signs, Inc.*, 183 F.3d 1347, 1356, 51 USPQ2d 1415, 1420 (Fed. Cir. 1999). However, "[a]s long as some motivation or suggestion to combine the references is provided by the prior art taken as a whole, the law does not require that the references be combined for the reasons contemplated by the inventor." *In re Beattie*, 974 F.2d 1309, 1312, 24 USPQ2d 1040, 1042 (Fed. Cir. 1992). Motivation to combine references under 35 U.S.C. § *103* must come from a teaching or suggestion within the prior art, within the nature of the problem to be solved, or within the general knowledge of a person of ordinary skill in the field of the invention, to look to particular sources, to select particular elements, and to combine them as combined by the inventor. *Ruiz v. A.B. Chance Co.*, 234 F.3d 654, 665, 57 USPQ2d 1161, 1167 (Fed. Cir. 2000).

> "[A]n implicit motivation to combine exists not only when a suggestion may be gleaned from the prior art as a whole, but when the 'improvement' is technology-independent and the combination of references results in a product or process that is more desirable, for example because it is stronger, cheaper, cleaner, faster, lighter, smaller, more durable, or more efficient . . . . In such situations, the proper question is whether the ordinary artisan possesses knowledge and skills rendering him *capable* of combining the prior art references." *DyStar Textilfarben GmbH & Co. Deutschland KG v. C.H. Patrick Co.*, 464 F.3d 1356, 1368, 80 USPQ2d 1641, 1651 (Fed. Cir. 2006).

ANALYSIS

Since we find that Appellants have elected not to appeal the Examiner's rejection of claims 1-3, 6-13, 16-18 under the judicially doctrine

of obviousness double patenting as being unpatentable over claims 1-16 of Hannum, we therefore affirm pro forma the double patenting rejection of claims 1-3, 6-13 and 16-18.

Next, we find that Miller teaches the invention as recited in representative claim 1. We note that, at initialization, Miller populates the ACAM with invalid states while the claimed invention populates the cache with illegal values. We also note that both Miller and the claimed invention populate their respective tables as indicated for the purpose of preventing a possible match between such values and prospective value entries. Additionally, we note that both the illegal values used in the claimed invention and Miller's invalid states are obtained at initialization (i.e. not obtained during the normal course of program execution). Therefore, we are persuaded by the weight of the evidence before us that Miller's teaching of populating the ACAM with illegal states, at initialization, teaches Appellants' claim limitation of populating of the associative table with illegal values. Thus, after considering the entire record before us, we find that the Examiner did not err in rejecting claims 1, 2, 7, 8, 10 through 12 and 17 through 19 as being anticipated by Miller.

Next, we find that that the Examiner properly found the motivation in the references themselves to combine the disclosures of Miller and Geva or Hale to yield the invention, as recited in claims 3, 6, 9, 13, and 16. We note in the findings of fact above that Geva teaches an advanced load address table (ALAT) that interacts with an advance load or advance load check that causes a processor to perform a load from a memory location. Particularly, Geva suggests that such an approach can be used to invalidate overlapping

regions of memory during a computer software optimization. One of ordinary skill in the art, at the time of the invention, would have readily recognized that Geva's suggested approach for invalidating a particular region in memory would optimize Miller's invalidation operation by pre-screening the status bits in the ACAM at initialization. Similarly, we find that the ordinary skilled artisan would have readily recognized that Hale's teaching of securing the invalidating a portion of a cache following a write back invalidate instruction during initialization would enhance the security of Miller's invalidation operation. Consequently, unauthorized codes such as viruses would not be able to interfere with Miller's invalidation operation during the initialization process. After considering the entire record before us, we find that the Examiner did not err in rejecting claims 3, 6, 9, 13, and 16 over Miller in combination with Geva or Hale.

CONCLUSION OF LAW

On the record before us, Miller anticipates the claimed invention under 35 U.S.C. § 102 (b) when Miller discloses Miller discloses initializing all valid status bits to an invalid state. Further, one of ordinary skill in the art at the time of the present invention, would have found sufficient motivation under 35 U.S.C. § 103 to combine Geva or Hale with Miller by incorporating a most recent advanced load instruction for a check instruction or a specific machine for executing writing instructions in an architecture for implementing invalid data.

DECISION

We affirmed the Examiner's decision to reject claims 1-3, 6-13 and 16-18 under obviousness double patenting. We have also affirmed the Examiner's decision to reject claims 1, 2, 7, 8, 10 through 12 and 17 through

19 under 35 U.S.C. § 102. Additionally, we have affirmed the Examiner's decision to reject claims 3, 6, 9, 13, and 16 under 35 U.S.C. § 103.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

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